JESD204B Clock Generator with 8 Outputs

FEATURES

- 8 outputs configurable for LVCMOS, LVDS, LVPECL and HSTL
- Maximum Output Frequency: 8 outputs up to 1.25GHz
- Dependent on the voltage controlled crystal oscillator (VCXO) frequency accuracy (start-up frequency accuracy: < ±100ppm)
- Dedicated 8-bit dividers on each output
  - Coarse Delay: 63 steps at 1/2 the period of the RF VCO divider output frequency with no jitter impact
  - Fine Delay: 15 steps of 22ps resolution
- Typical output to output skew: 20ps
- Duty cycle correction for odd divider settings
- Absolute output jitter: < 160fs at 122.88MHz, 12KHz to 20MHz integration range
- Digital frequency lock detect
- SPI- and I^2C-compatible serial control port
- Dual PLL architecture: PLL1 and PLL2
- PLL1
  - Provides reference input clock cleanup with external VCXO
  - Phase detector rate up to 110MHz
  - Redundant Reference Inputs
  - Automatic and manual reference switchover modes
  - Loss of reference detection with holdover mode
  - Low noise LVDS/HSTL outputs from VCXO used for radio frequency/intermediate frequency (RF/IF) synthesizers
- PLL2
  - Phase detector rate of up to 275MHz
  - Integrated low noise VCO
- Humidity sensitivity level
  - MSL-1 and MSL-3 optional

APPLICATIONS

- High performance wireless transceivers
- LTE and Multicarrier GSM base stations
- Wireless and broadband infrastructure
- Medical Instrumentation
- Clocking high speed ADCs, DACs, DDSs, supports JESD204B
- Low jitter, low phase noise clock distribution
- ATE and high performance instrumentation

GENERAL DESCRIPTION

The GM5508 is a two-stage PLL with an integrated JESD204B SYSREF generator for multiple devices synchronization. The first stage phase-locked loop (PLL) (PLL1) provides input reference conditioning by reducing the jitter present on a system clock. The second stage PLL (PLL2) provides high frequency clocks that achieve low integrated jitter as well as low broadband noise from the clock output dividers. The external VCXO provides the low noise reference required by PLL2 to achieve the restrictive phase noise and jitter requirements necessary to achieve acceptable performance. The on-chip VCO tunes from 3.6GHz to 3.95GHz. The integrated SYSREF generator outputs single shot, N-shot, or continuous signals synchronous to the PLL1 and PLL2 outputs to time align multiple devices.

The GM5508 generates 8 outputs up to 1.25GHz. Each output can be configured to output directly from PLL1, PLL2 and the internal SYSREF generator. Each of the 8 output channels contains a divider with coarse digital phase adjustment and an analog fine phase delay block that allows complete flexibility in timing alignment across all 8 outputs. The GM5508 can also be used as a dual input flexible buffer to distribute 8 device clock and/or SYSREF signals.

FUNCTIONAL BLOCK DIAGRAM

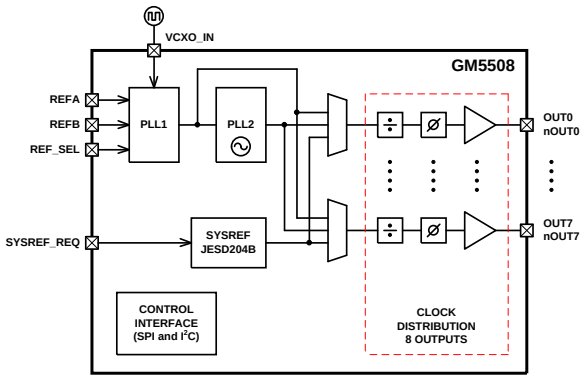

Figure 1, Functional Block Diagram

PIN CONFIGURATION (QFN72-10x10mm)

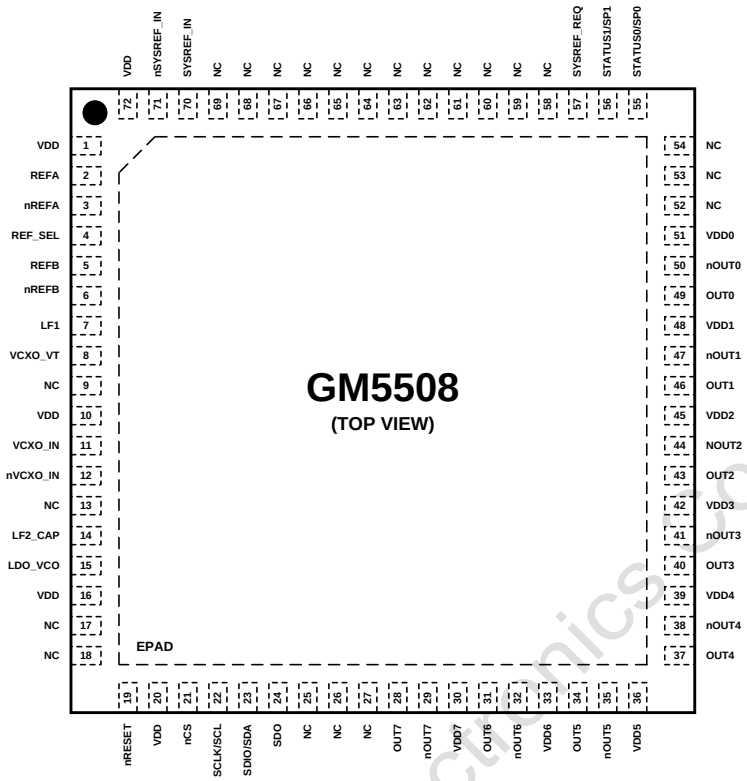

Figure 2, Pin Configuration

PIN FUNCTION DESCRIPTIONS

PIN NO.	PIN NAME	TYPE(1)	DESCRIPTIONS
1	VDD	P	3.3V Supply for the PLL1 Input Section.
2	REFA	I	Reference Clock Input A. Along with nREFA, this pin is the differential input for the PLL reference. Alternatively this pin can be programmed as a single-ended 3.3V CMOS input.
3	nREFA	I	Complementary Reference Clock Input A. Along with REFA, this pin is the differential input for the PLL reference. Alternatively this pin can be programmed as a single-ended 3.3V CMOS input.
4	REF_SEL	I	Reference Input Select. The reference input selection function defaults to software control via Register 0x0101, Bits[7]. When the REF_SEL pin is active, a logic Low selects REFA and logic High selects REFB.
5	REFB	I	Reference Clock Input B. Along with nREFB, this pin is the differential input for the PLL reference. Alternatively this pin can be programmed as a single-ended 3.3V CMOS input.
6	nREFB	I	Complementary Reference Clock Input B. Along with REFB, this pin is the differential input for the PLL reference. Alternatively this pin can be programmed as a single-ended 3.3V CMOS input.
7	LF1	O	PLL1 External Loop Filter.
8	VCXO_VT	O	VCXO Control Voltage. Connect this pin to the voltage control pin of the external VCXO.
9	NC	NC	No Internal Connection. This pin can be left floating.
10	VDD	P	3.3V Supply for the PLL2 Section.
11	VCXO_IN	I	PLL1 Oscillator Input. Along with nVCXO_IN, this pin is the differential input for the PLL reference. Alternatively this pin can be programmed as a single-ended 3.3V CMOS input.